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Michael J. Mallie
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
HABTE, ZEWDU	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,379	ALI ET AL.	
	Examiner	Art Unit	
	Zewdu Habte	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7,9,10,12-15,17,18,20-23,25 and 26 is/are rejected.

7)☒ Claim(s) 8,11,16,19,24,27 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9,10,12-15,17,18,20-23,25,26 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoh et al. (5305310).

As to claim 1 Itoh discloses a method for selecting packets, comprising: pipelining execution of packet selection processes so that execution of each of the packet selection processes occurs at different levels of a scheduling hierarchy (col. 1, lines 59-68, packets entered into the highest positioned of sorting module; the sorting module peeks one of the competing packets, and drops the rest of the packets to the second highest positioned of the sorting module); and selecting at least two different packets at two different times in response to execution of the packet selection processes (col. 1, lines 59-68, these packets are selected at two different times; the first packet selection is done in the first process, then the second process for the second packet selection proceeds).

As to claim 2 Itoh discloses the method of claim 1, wherein each of the packet selection processes comprises two or more sub processes executed at different levels

of the scheduling hierarchy to select a packet (col. 2, lines 15-18, packets are entered at the same module with a predefined delay, and the selection process starts at the highest module to the lowest; in each module each packet goes through a sub process for a selection).

As to claim 3 Itoh discloses the method of claim 2, wherein pipelining execution of the packet selection processes comprises executing each of the packet selection processes independent of on another (the process of packet selection is done in the highest sorting module, it is independent of the process of packet selection done in the second highest module).

As to claims 4 and 12 Itoh discloses a method for selecting packets comprising: initiating a first packet selection process at a first time slot (col. 4, lines 35-67, first the plurality of packets entered into the packet switching system are inputted to the sorting system; col. 4, lines 19-22, ...a timing pulse 112, a first time slot, Fig. 1 @ 112), initiating a second packet selection process at a second time slot immediately following the first time slot such that execution of the second packet selection process overlaps execution of the first packet selection process at different levels of a scheduling hierarchy (col. 3, lines 14-17, on the other hand, ...the packets P1 and P3 are competing with each other in Sorting Module 12 and packet P3 has a priority; col. 4, lines 19-22, ...a timing pulse 115, second time slot, but the process to forward packets P1 and P3 to Sorting Module 12 started at the first time slot when the decision process began by Dropping Circuit 4 in Sorting Module 11); selecting a first packet at a third time slot in response to the first packet selection process (col. 3, lines 30-34, the kept packet

is output to n-data lines 103; col. 4, lines 19-22, ... a timing pulse 113, third time slot, Fig. 1 @ 113); and selecting a second packet at a fourth time slot in response to the second packet selection process, the fourth time slot immediately following the third time slot (col. 3, lines 30-34, the kept packet is output to n-data lines 103; col. 4, lines 19-22, ... a timing pulse before the routing circuit 5 in module 12, the fourth time slot; this is the same reasoning used above for module 11, except this time it is used for module 12; the timing slot before sorting circuit 3 is the second time slot 115; then the pulse before dropping circuit 4 is the third time slot, and the pulse before routing circuit 5 is the fourth time slot and the second packet P3 is selected there).

As to claims 5 and 13 Itoh discloses the method of claim 4, wherein each of the first packet selection process and the second packet selection process comprises two or more sub processes executed to select the first packet and the second packet respectively (Fig. 1 @ module 11, dropping circuit comprising a competition arbitrative circuit, 411, 412,...41n; col. 3, lines 59-68, the competition arbitrative circuits 411 to 41n determine whether or not a given packet is to be dropped; if the packet wins the competition, there is a transfer to the output line 103, which is to say, execute the first packet process; otherwise, the packet is dropped to the lowest position through line 410).

As to claims 6 and 14 Itoh discloses the method of claim 5, wherein each of the two or more sub processes in the first packet selection process and in the second packet selection process is executed in one time slot (col. 4, lines 19-22, says every time a process is completed at one of the three circuits, a timing pulse is supplied to the

packet's starting position and this forwards the packet to the next line; in this case, until the dropping circuit's process is done, the timing pulse that attached to this process is 112, and it is one time slot).

As to claims 7 and 15 Itoh discloses the method of claim 6, wherein each of the two or more sub processes in the first packet selection process and in the second packet selection process is executed at a different level of the scheduling hierarchy (col. 3, lines 59-61, the competition arbitrative circuits 411 to 41n determine whether or not a given packet is to be dropped; circuit 411 is in the highest position, and the circuit 41n in the lowest position; the packet with circuit number 411 has highest priority, and the packet with circuit number 41n has lowest priority).

As to claims 9 and 17 Itoh discloses the method of claim 5, wherein when a sub process is selected by the first packet selection process, it is locked and cannot be selected by the second packet selection process (col. 3, lines 33-38, the kept packet and non-competing packets are output to n-data lines 103; once the packet is selected, it is moved to the routing circuit 5 which is to show there is no second packet selection process on that particular packet; col. 4, lines 66-68, otherwise the packet will survive; surviving packets, which either are non-competing or have won the competition).

As to claims 10 and 18 Itoh discloses the method of claim 9, wherein the sub process is selected from one or more sub processes at a same level of the scheduling hierarchy by sorting the one or more sub processes at that level based on a selection criteria (col. 4, lines 56-67, then, the sorted packets are entered into the competition-arbitrative sections 41 of the dropping circuit 4; in each of the competition-arbitrative

circuits 412 to 41n...; its address is compared with that of the packet entered from the data line 102; if the packet is found to have the same address as the packet which is superior in the sorting order, it will be considered defeated in the competition).

As to claim 20 Itoh discloses a system comprising: a switch fabric (Fig.1); and an egress coupled with the switch fabric (Fig. 1 @101) to: initiate a first packet selection process at a first time slot (col. 4, lines 35-67, first the plurality of packets entered into the packet switching system are inputted to the sorting system; col. 4, lines 19-22, ...a timing pulse 112, a first time slot, Fig. 1 @ 112), initiate a second packet selection process at a second time slot immediately following the first time slot such that execution of the second packet selection process overlaps execution of the first packet selection process at different levels of a scheduling hierarchy (col. 3, lines 14-17, on the other hand, ...the packets P1 and P3 are competing with each other in Sorting Module 12 and packet P3 has a priority; col. 4, lines 19-22, ...a timing pulse 115, second time slot, but the process to forward packets P1 and P3 to Sorting Module 12 started at the first time slot when the decision process began by Dropping Circuit 4 in Sorting Module 11); select a first packet at a third time slot in response to the first packet selection process (col. 3, lines 30-34, the kept packet is output to n-data lines 103; col. 4, lines 19-22, ... a timing pulse 113, third time slot, Fig. 1 @ 113); and select a second packet at a fourth time slot in response to the second packet selection process, the fourth time slot immediately following the third time slot (col. 3, lines 30-34, the kept packet is output to n-data lines 103; col. 4, lines 19-22, ... a timing pulse before the routing circuit 5 in module 12, the fourth time slot; this is the same reasoning used above for module

11, except this time it is used for module 12; the timing slot before sorting circuit 3 is the second time slot 115; then the pulse before dropping circuit 4 is the third time slot, and the pulse before routing circuit 5 is the fourth time slot and the second packet P3 is selected there).

As to claim 21 Itoh discloses the system of claim 20, wherein each of the first packet selection process and the second packet selection process comprises two or more sub processes executed to select the first packet and the second packet respectively (Fig. 1 @ module 11, dropping circuit comprising a competition arbitrative circuit, 411, 412,...41n; col. 3, lines 59-68, the competition arbitrative circuits 411 to 41n determine whether or not a given packet is to be dropped; if the packet wins the competition, there is a transfer to the output line 103, which is to say, execute the first packet process; otherwise, the packet is dropped to the lowest position through line 410).

As to claim 22 Itoh discloses the system of claim 21, wherein each of the two or more sub processes in the first packet selection process and in the second packet selection process is executed in one time slot (col. 4, lines 19-22, says every time a process is completed at one of the three circuits, a timing pulse is supplied to the packet's starting position and this forwards the packet to the next line; in this case, until the dropping circuit's process is done, the timing pulse that attached to this process is 112, and it is one time slot).

As to claim 23 Itoh discloses the system of claim 22, wherein each of the two or more sub processes in the first packet selection process and in the second packet

selection process is executed at a different level of the scheduling hierarchy (col. 3, lines 59-61, the competition arbitrative circuits 411 to 41n determine whether or not a given packet is to be dropped; circuit 411 is in the highest position, and the circuit 41n in the lowest position; the packet with circuit number 411 has highest priority, and the packet with circuit number 41n has lowest priority).

As to claim 25 Itoh discloses the system of claim 21, wherein when a sub process is selected by the first packet selection process, it is locked and cannot be selected by the second packet selection process (col. 3, lines 33-38, the kept packet and non-competing packets are output to n-data lines 103; once the packet is selected, it is moved to the routing circuit 5 which is to show there is no second packet selection process on that particular packet; col. 4, lines 66-68, otherwise the packet will survive; surviving packets, which either are non-competing or have won the competition).

As to claim 26 Itoh discloses the system of claim 25, wherein the sub process is selected from one or more sub processes at a same level of the scheduling hierarchy by sorting the one or more sub processes at that level based on a selection criteria (col. 4, lines 56-67, then, the sorted packets are entered into the competition-arbitrative sections 41 of the dropping circuit 4; in each of the competition-arbitrative circuits 412 to 41n...; its address is compared with that of the packet entered from the data line 102; if the packet is found to have the same address as the packet which is superior in the sorting order, it will be considered defeated in the competition).

Allowable Subject Matter

Claims 8, 11, 16, 19, 24 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zewdu Habte whose telephone number is 571-272-3115. The examiner can normally be reached on 8:30-5:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zewdu Habte

December 6, 2004

KENNETH VANDERPUYE
PRIMARY EXAMINER